**SPI (Serial Peripheral Interface)**

**🔹 Overview**

* **SPI = Serial Peripheral Interface**
* **4-wire communication bus**, widely used in embedded systems.
* **Faster than UART & I²C**, typically in the **MHz range**.
* **Full-duplex** supported (send & receive simultaneously).
* **Loosely defined** standard → implementations may vary.
* Common in **ADC, DAC, displays, memory chips**.

**🔹 Protocol Basics**

* **Master–Slave protocol**
  + **Single master (controller)**
  + **Multiple peripherals (slaves)**
* Up to **4 wires**:
  + **SCLK (Serial Clock)** – provided by master
  + **MOSI (Master Out Slave In)** – master sends data
  + **MISO (Master In Slave Out)** – slave sends data
  + **CS/SS (Chip Select / Slave Select)** – master selects target (active LOW)

📍 **Key:** Master pulls CS low → starts clock → data exchange → CS pulled high at end.

**🔹 Signal Descriptions**

**1. SCLK**

* Clock generated by master.
* Defines **bit timing**: 1 clock = 1 bit.
* Idle state can be HIGH or LOW (configurable via **CPOL**).
* Data sampled on **rising or falling edge** (via **CPHA**).

**2. MOSI**

* Data from master → slave.
* Transmitted in **bytes** (LSB-first or MSB-first depending on config).

**3. MISO**

* Data from slave → master.
* Not always used (e.g., display writes → 3-wire SPI).

**4. CS / SS**

* Active **LOW** (0 = selected).
* One CS per slave (multi-slave independent).
* Alternative: **Daisy Chain** (shared CS + serial pass-through).

**🔹 SPI Modes (Clock Polarity & Phase)**

Two config bits:

* **CPOL (Clock Polarity):**
  + 0 → Clock idle LOW, leading edge = rising
  + 1 → Clock idle HIGH, leading edge = falling
* **CPHA (Clock Phase):**
  + 0 → Sample on leading edge
  + 1 → Sample on trailing edge

**Mode Table**:

| **Mode** | **CPOL** | **CPHA** | **Idle** | **Sample Edge** |
| --- | --- | --- | --- | --- |
| 0 | 0 | 0 | Low | Rising |
| 1 | 0 | 1 | Low | Falling |
| 2 | 1 | 0 | High | Falling |
| 3 | 1 | 1 | High | Rising |

⚠️ **All devices must use the same SPI mode.**

**🔹 Multi-Slave Configurations**

**1. Independent Slaves**

* Each slave has its **own CS line**.
* Master controls which slave is active.

**2. Daisy Chain (Cooperative Slaves)**

* Slaves connected in series.
* Data flows: Master → Slave1 (MOSI) → Slave2 → Slave3 …
* Useful when pin count must be minimized.

**🔹 Key Takeaways**

* SPI is **fast, simple, full-duplex**, but not standardized (implementation details vary).
* **CPOL & CPHA** must be set correctly on both master & slave.
* **CS line** determines which slave is active.
* Used heavily in **sensors, displays, ADC/DAC, memories**.